AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (previously presented) A method for cleaning a wafer, comprising:

patterning a via or a trench, or both, in a porous, low-k dielectric layer overlying the wafer;

cleaning a polymer residue from surfaces of the patterned dielectric layer using a wet clean solvent;

performing a non-plasma anneal on the patterned dielectric layer to remove a component of the solvent prior to a metal deposition, wherein the anneal comprises a low pressure anneal from about one atmosphere of pressure to substantial vacuum; and

after an anneal duration of about six minutes or less, stopping the anneal.

2. (previously presented) The method of claim 1, wherein the dielectric layer comprises at least one of: an organosilicate glass (OSG), a methylsilsesquioxane (MSQ) dielectric material, a fluorine-doped silicate glass (FSG), and a silicon-dioxide (SiO2).

3. (previously presented) The method of claim 1, wherein the wet clean solvent comprises an acid.

4. (previously presented) The method of claim 3, wherein the component comprises dimethyl acetamide (DMAC).

5. (previously presented) The method of claim 1, further comprising:

performing a dry clean of the patterned dielectric layer to remove a photoresist, prior to cleaning the polymer residue.

6. (previously presented) The method of claim 5, wherein the dry clean comprises a plasma including at least one of: hydrogen, oxygen and an inert gas.

7. (canceled)

8. (previously presented) The method of claim 1, wherein the low-pressure anneal is performed in substantially a vacuum.

9. (previously presented) The method of claim 1, wherein the anneal comprises a high-temperature anneal.

10. (previously presented) The method of claim 9, wherein the high-temperature anneal is performed at a higher temperature than a boiling point of the component.

11. (previously presented) The method of claim 9, wherein the high temperature anneal is performed at a temperature less than or equal to 300 degrees Celsius.

12. (previously presented) The method of claim 9, wherein the high temperature anneal is at least partially performed at 250 degrees Celsius.

13. (previously presented) The method of claim 1, wherein the anneal is performed for a duration that does not alter a critical dimension of the patterned dielectric layer and does not cause a metal extrusion.

14. (previously presented) The method of claim 13, wherein the duration comprises at most three minutes.

15. (previously presented) The method of claim 1, wherein the anneal excludes an application to the patterned dielectric layer of a plasma generated from at least one of: a radio-frequency energy and a microwave energy.

16. (canceled)

17. (previously presented) The method of claim 1, wherein the metal deposition includes a copper deposition.

18. (previously presented) The method of claim 1, wherein the metal deposition comprises at least one of: a barrier deposition and a metal seed layer deposition.

19. (canceled)

20. (withdrawn) A method for removing volatile cleanser compounds from a post-etch substrate, comprising:

performing a plasma strip of an exposed low-k dielectric material to remove a photoresist residue after an etch of the material;

performing a wet clean process using a fluorine-based solvent to remove a polymer residue of the plasma strip from the material;

performing an anneal at a pressure of about one atmosphere or less and a temperature of between about 250°C and about 300°C after the wet clean process and prior to a metal barrier deposition to remove a component of the fluorine-based solvent

from the material, wherein the anneal is exclusive of an application of a plasma generated from one or more of: a radio-frequency (RF) radiation and a microwave radiation; and

after an anneal duration of about six minutes or less, stopping the anneal.

21. (withdrawn) A method used during fabrication of a semiconductor device, comprising:

patterning a via or a trench, or both, in a low-k dielectric layer comprising organosilicate glass (OSG);

cleaning a polymer residue from a surface of the patterned dielectric layer using a wet clean solvent; and

performing a non-plasma anneal on the patterned dielectric layer at a temperature of about 250°C for a duration of about 45 seconds.

22. (withdrawn) The method of claim 21 further comprising performing the anneal at a pressure of about one atmosphere or less.

23. (withdrawn) The method of claim 21 further comprising performing the non-plasma anneal to remove a component of the wet clean solvent.

24. (new) The method of claim 1, further comprising depositing a metal layer into the via or trench, or both, wherein the patterned via or trench, or both, is not subjected to a powered plasma before depositing the metal layer.

25. (new) The method of claim 1 wherein the anneal is performed at a temperature of about 250°C for a duration of about 45 seconds.